EXHIBIT 2

U.S. Patent No. 8,549,339 ("'339 Patent")

Accused Products

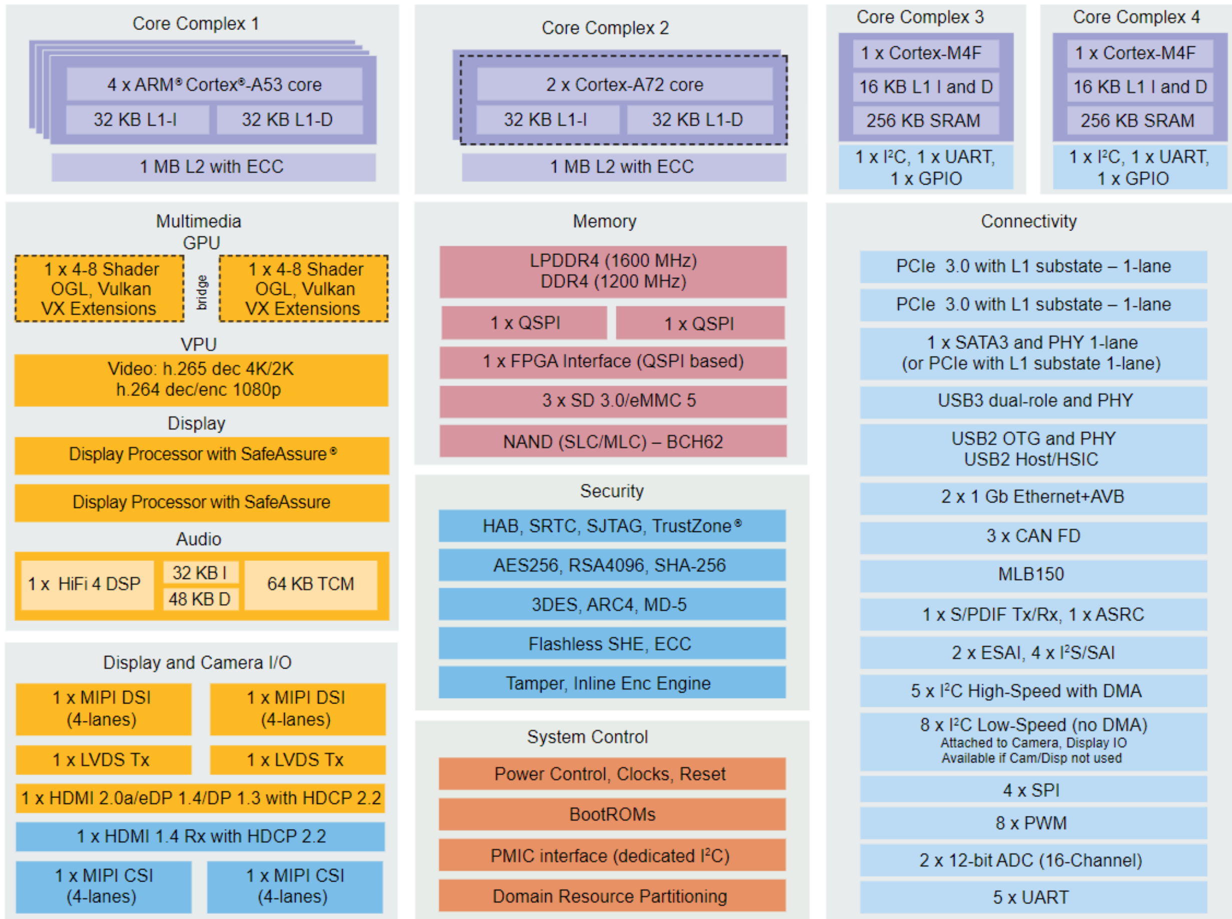
NXP's products comprising two or more sets of processors supporting or based on the ARM big.LITTLE architecture, including without limitation the NXP i.MX 8 Family Application Processors, and all variants and iterations thereof, including without limitation any non-public NXP products comprising two or more sets of processors in a big.LITTLE configuration (collectively, "Accused Products"), infringe at least Claims 1, 5, 8, 9, 10, 14, and 21 of the '339 Patent.

Each Accused Product infringes the claims in substantially the same way, and the evidence shown in this chart is similarly applicable to each Accused Product. For example, each Accused Product includes a big.LITTLE architecture and, on information and belief, implements substantially the same architectural features described in the reference documentation cited in this chart. The NXP document "IMX8QM1P3AEC" cited below is exemplary of the i.MX 8 Family products. Thus, the descriptions and evidence below relating to the NXP i.MX 8 Family Application Processor representative products are similarly applicable to the remaining Accused Products listed above. Each claim limitation is literally infringed by each Accused Product. However, to the extent any claim limitation is not met literally, it is nonetheless met under the doctrine of equivalents because the differences between the claim limitation and each Accused Product would be insubstantial, and each Accused Product performs substantially the same function, in substantially the same way, to achieve the same result as the claimed invention. Notably, Defendant has not yet articulated which, if any, particular claim limitations it believes are not met by the Accused Products.

Claim 1

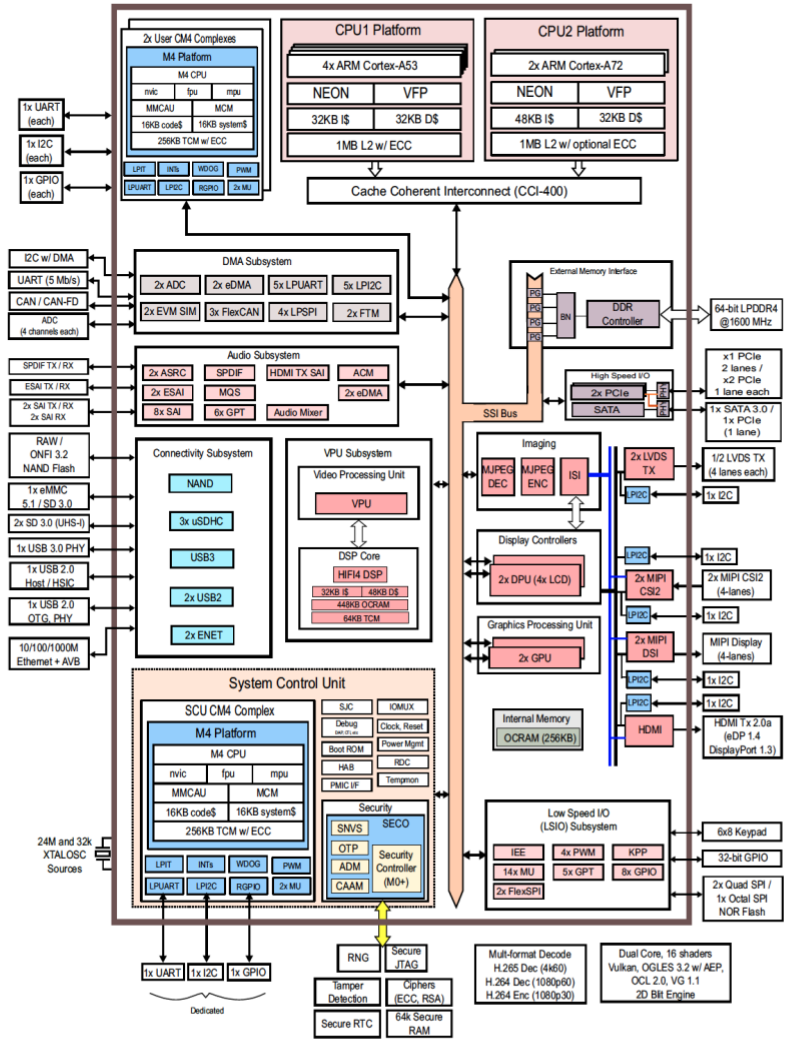
Claim 1	Accused Products
1. A multi-core processor, comprising:	To the extent the preamble is limiting, each Accused Product comprises a multi-core processor. For example, the NXP i.MX 8 Family Application Processor contains six cores implementing the ARM big.LITTLE architecture. *See, e.g.*:

Claim 1	Accused Products
[1b] a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and	Each Accused Product comprises a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal. For example, in addition to the first set of processor cores, the NXP i.MX 8 Family Application Processor includes a second core complex with 2 ARM Cortex-A72 cores. The processor cores in the second set receive a second, independent dynamic supply voltage and a second, independent clock signal of a second PLL. ARM documentation for the big.LITTLE architecture used in the i.MX 8 Family Application Processor directly shows that each core cluster (*e.g.*, the Core Complex 2 containing 2 ARM Coretex-A72 cores) receives its own clock domain. At the time the i.MX 8 Family Application Processor was designed, it was typical to produce this clock using a PLL that has a corresponding clock input. Furthermore, ARM documentation for an earlier, related device (the Cortex-A15_A7 MPCore test chip, which also has independent clock domains for different CPU clusters) shows each CPU cluster receiving an output clock signal from a PLL having a corresponding clock signal as input (*e.g.* from an oscillator). It is therefore substantially likely that the i.MX 8 Family Application Processor specifically receives a first output clock signal of a first PLL having a first clock signal as input. *See, e.g.*:

<table>
<tr><th>Claim 1</th><th>Accused Products</th></tr>
<tr><td></td><td>


https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-applications-processors/i-mx-8-family-arm-cortex-a53-cortex-a72-virtualization-vision-3d-graphics-4k-video:i.MX8
</td></tr>
</table>

Claim 1	Accused Products
	Features **Processor Complex** • Core Complex #1: 4x Cortex-A53 • Core Complex #2: 2x Cortex-A72 • 2x Cortex-M4F • 1x HIFI4 DSP https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-applications-processors/i-mx-8-family-arm-cortex-a53-cortex-a72-virtualization-vision-3d-graphics-4k-video:i.MX8

Claim 1	Accused Products
	 **Figure 1. i.MX 8QuadMax System Block Diagram** https://www.nxp.com/docs/en/data-sheet/IMX8QM1P3AEC.pdf

Claim 1	Accused Products
	(see tables below)

Parameter Description	Symbol	Min	Max	Units
Core Supplies Input Voltage	VDD_A72	-0.3	1.2	V
	VDD_A53			
	VDD_GPU0			
	VDD_GPU1			
	VDD_MAIN			
	VDD_MEMC			

https://www.nxp.com/docs/en/data-sheet/IMX8QM1P3AEC.pdf

Table 8. Operating ranges[1]

Symbol	Description	Mode	Min	Typ	Max	Unit	Comments
VDD_A72	Power supply of Cortex-A72 cluster	Overdrive	1.05	1.10	1.15	V	Min frequency = 208.5 MHz Max frequency = 1.296 GHz
		Nominal	0.95	1.00	1.10	V	Max frequency = 1.06 GHz
VDD_A53	Power supply of Cortex-A53 cluster	Overdrive	1.05	1.10	1.15	V	Min frequency = 208.5 MHz Max frequency = 1.2 GHz
		Nominal	0.95	1.00	1.10	V	Max frequency - 900 MHz

https://www.nxp.com/docs/en/data-sheet/IMX8QM1P3AEC.pdf

Claim 1	Accused Products
	4.1.4 External clock sources Each processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI). The RTC_XTALI is used for real time functions. It supplies the clock for real time clock operation and for slow-system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input requires a crystal using the internal oscillator amplifier. The PCIe oscillator can be sourced internally or input to the chip. In both cases, it is a 100 MHz nominal clock using HCSL signaling to provide the PCIe reference clock. https://www.nxp.com/docs/en/data-sheet/IMX8QM1P3AEC.pdf

Claim 1	Accused Products
	Table 9. External Input Clock Frequency Parameter Description | Symbol | Min | Typ | Max | Unit RTC_XTALI Oscillator[1,2] | f_{ckil} | — | 32.768[3]/32.0 | — | kHz XTALI Oscillator[4,2] | f_{xtal} | — | 24 | — | MHz PCIe oscillator[5] | f_{100M} | — | 100 | — | MHz Frequency accuracy | — | — | — | ±300 | ppm 1 External oscillator or a crystal with internal oscillator amplifier. 2 The required frequency stability of this clock source is application dependent. For recommendations, see the hardware development guide for this device. 3 Recommended nominal frequency 32.768 kHz. 4 Fundamental frequency crystal with internal oscillator amplifier. 5 If using an external clock instead of the internal clock source, an HCSL-compatible clock is required. Concerning EMI/EMC, note that internal source is not spread-spectrum capable. The typical values shown in Table 9 are required for use with NXP board support packages (BSPs) to ensure precise time keeping and USB and HDMI operations. https://www.nxp.com/docs/en/data-sheet/IMX8QM1P3AEC.pdf

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4.3 PLL electrical characteristics

4.3.1 PLLs of subsystems

i.MX 8QuadMax embeds a large number of PLLs to address clocking requirements of the various subsystems. These PLLs are controlled through the SCU and not directly by Cortex-A or Cortex-M4F processors. A software API shall be used by those processors to access the PLL settings. Additional PLLs are specific to high-performance interfaces. These are described in the following sections.

This table summarizes the PLLs controlled by the SCU.

Table 16. PLLs controlled by SCU

<table>
<tr><th rowspan="2">Subsystem</th><th rowspan="2">PLL usage</th><th rowspan="2">Source clock</th><th colspan="2">Locking range[1]</th><th rowspan="2">Unit</th></tr>
<tr><th>Min freq.</th><th>Max freq.</th></tr>
<tr><td>Cortex-A53</td><td>Subsystem</td><td>24</td><td>1250</td><td>2500</td><td>MHz</td></tr>
<tr><td>Cortex-A72</td><td>Subsystem</td><td>24</td><td>1250</td><td>2500</td><td>MHz</td></tr>
</table>

https://www.nxp.com/docs/en/data-sheet/IMX8QM1P3AEC.pdf
</td></tr>
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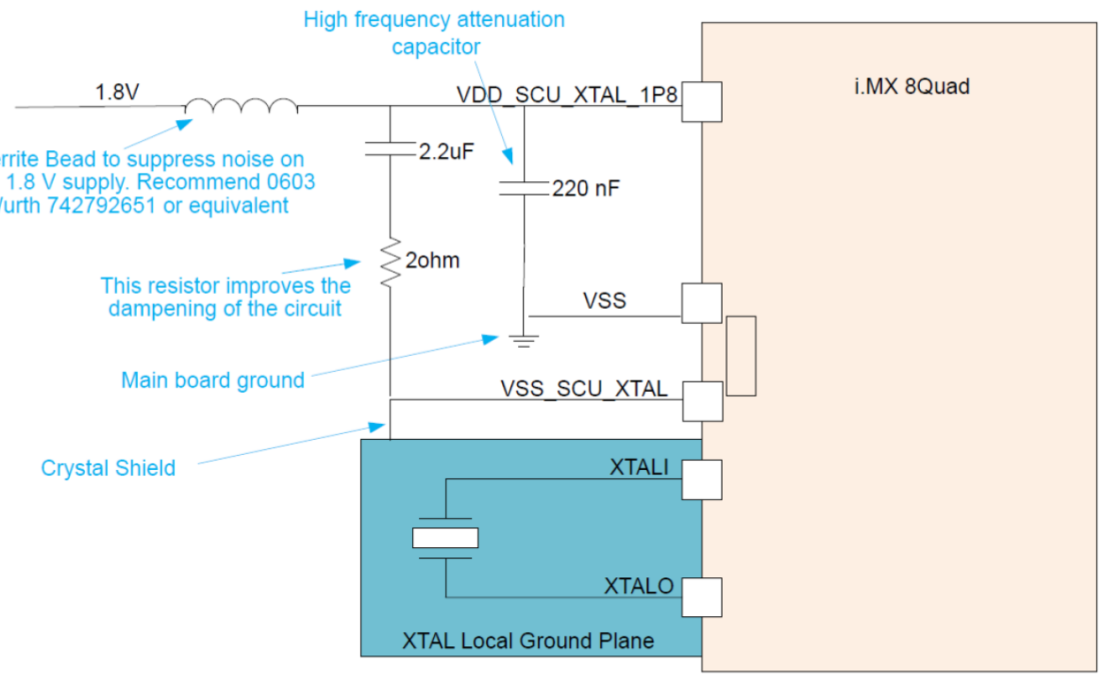
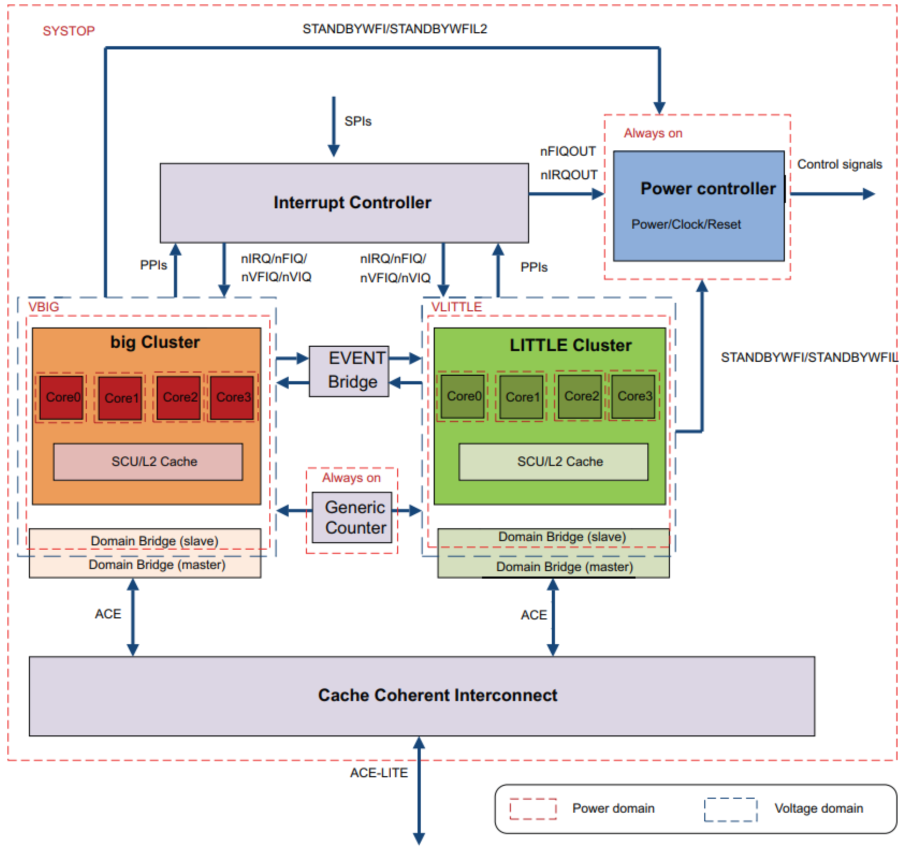
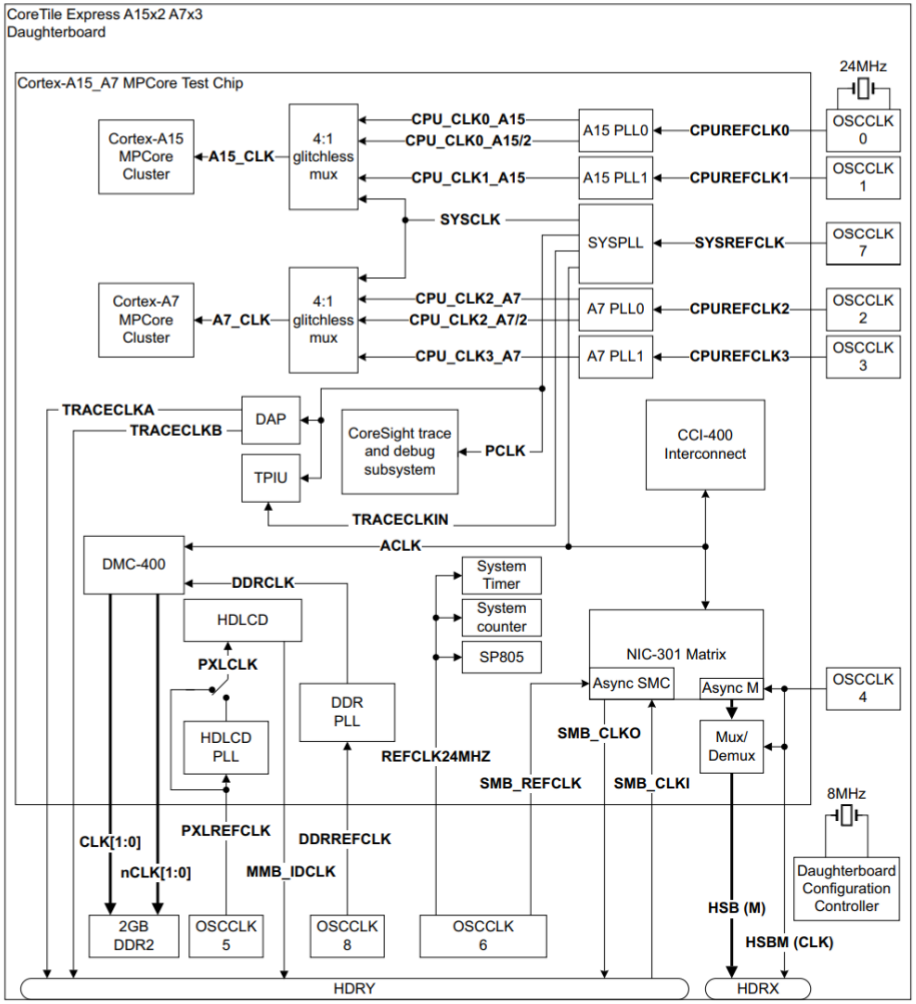
Claim 1	Accused Products
	4.4 On-chip oscillators **4.4.1 OSC24M** This block integrates trimmable internal loading capacitors and driving circuitry. When combined with a suitable 24 MHz external quartz element, it can generate a low-jitter clock. The oscillator is powered from VDD_SCU_XTAL_1P8. The internal loading capacitors are trimmable to provide fine adjustment of the 24 MHz oscillation frequency. It is expected that customers burn appropriate trim values for the selected crystal and board parasitics.  **Figure 2. Normal Crystal Oscillation mode** https://www.nxp.com/docs/en/data-sheet/IMX8QM1P3AEC.pdf

Claim 1	Accused Products
	Voltage domains The voltage supply to a domain might be scaled or removed for power or performance reasons. Except for low complexity solutions, it is rare to use a single logic voltage supply for the whole SoC. The primary reason for additional voltage domains is to support DVFS for functional areas of the SoC. The second reason is to enable external supply switch-off, or reduction to non-functional state retention levels, to some logic areas while maintaining an operational level supply to others. However, the cost for additional voltage domains is significant, because additional voltage regulators, extra effort, and complexity are required in the SoC physical implementation. Therefore, you must carefully assess the value of the addition of each voltage domain against the performance and power requirements for the design. In a big.LITTLE system, each cluster must have a dedicated voltage supply. This is a critical success factor when combined with big.LITTLE software. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	 **Figure 2-2 Power domain hierarchy** In Figure 2-2, two processor clusters are implemented with per-core and cluster power domains. The big cluster is in the VBIG voltage domain, while the LITTLE cluster is in the VLITTLE voltage domain. The system controller is in an always-on power domain. All the other components are in the system logic power domain (SYSTOP). "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	Clock domains Clock domains can interact with each other synchronously or asynchronously. Synchronous clock domains can have independent source activity. Each cluster requires an independent clock, and the CCI requires a clock. "High-level Considerations for Power Management of a big.LITTLE™ System Application Note 424," available at https://developer.arm.com/documentation/dai0424/a/

Claim 1	Accused Products
	 **Figure 2-10 CoreTile Express A15×2 A7×3 daughterboard clocks** ARM® CoreTile Express A15×2 A7×3 Technical Reference Manual, available at https://developer.arm.com/documentation/ddi0503/i/